# LQ4RE01/LQ4RE02
## TFT-LCD Module

### FEATURES

- TFT-Active Matrix Drive System
- 37,440 Pixels (Delta Configuration)
- Dual Mode Type (NTSC (M) and PAL (B, G))
- MBK-PAL, or MaBiKi-PAL, Which Enables the 234 Scan Line Panel to Display a Picture With Virtually 273 Scan Lines
- Slim, Lightweight and Compact:
  - Active Area/Outline Area: 41%
  - Thickness: 6.6 mm
  - Weight: 135 g
- Viewing Angle:
  - LQ4RE01: 6 O'Clock Direction
  - LQ4RE02: 12 O'Clock Direction

### DESCRIPTION

The SHARP LQ4RE01/LQ4RE02 Color TFT-LCD Module is an active matrix Liquid Crystal Display (LCD) produced by making the most of SHARP's expertise in liquid-crystal and semiconductor technologies. The active device is amorphous silicon Thin Film Transistor (TFT). The module accepts full color video signals conforming to both NTSC (M) and PAL (B, G) system standards.

The module consists of a TFT-LCD panel, driver ICs, control PWB, frames, and shielding cases (lid and rear).

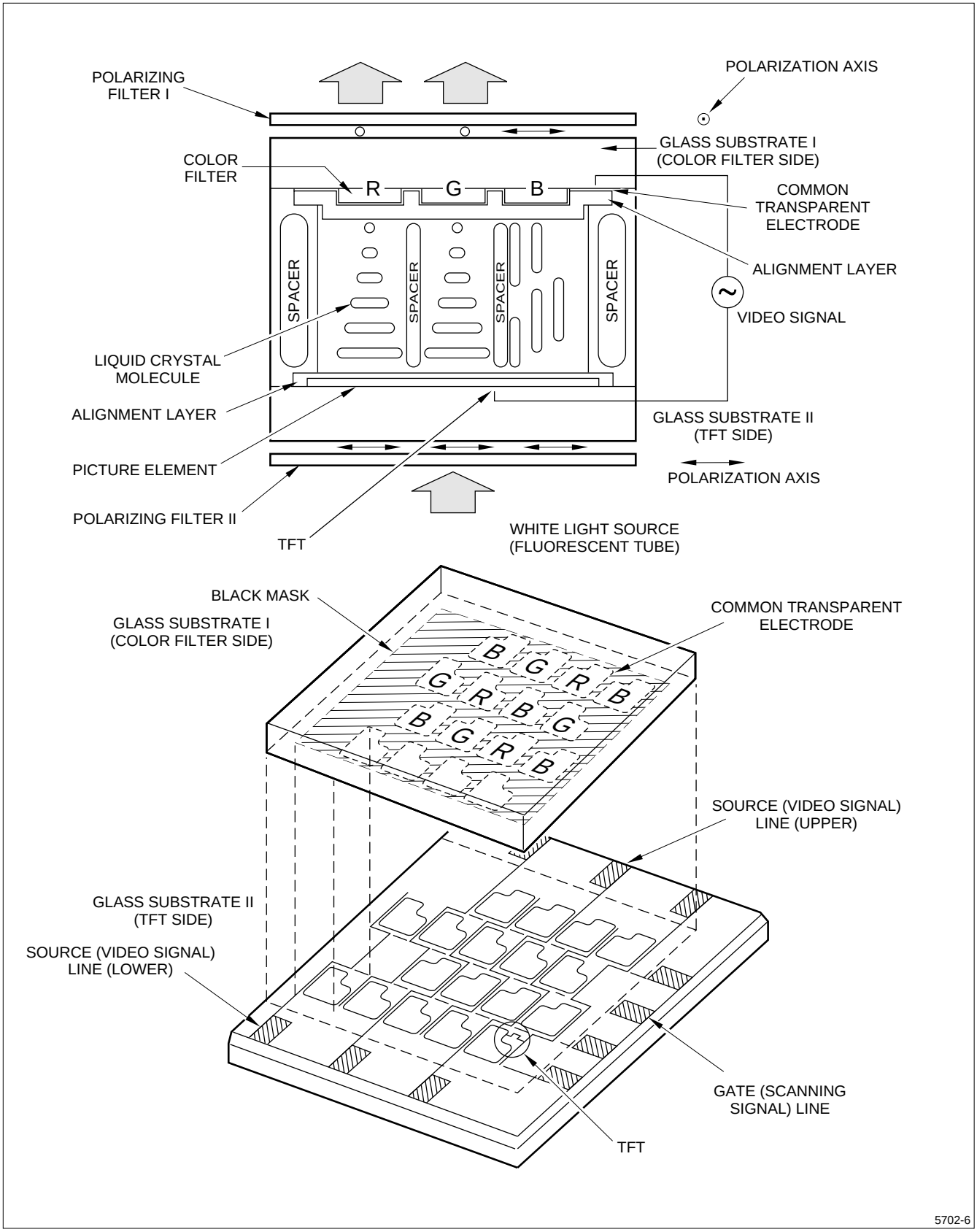



**Figure 1. LQ4RE01/LQ4RE02 TFT-LCD Panel**

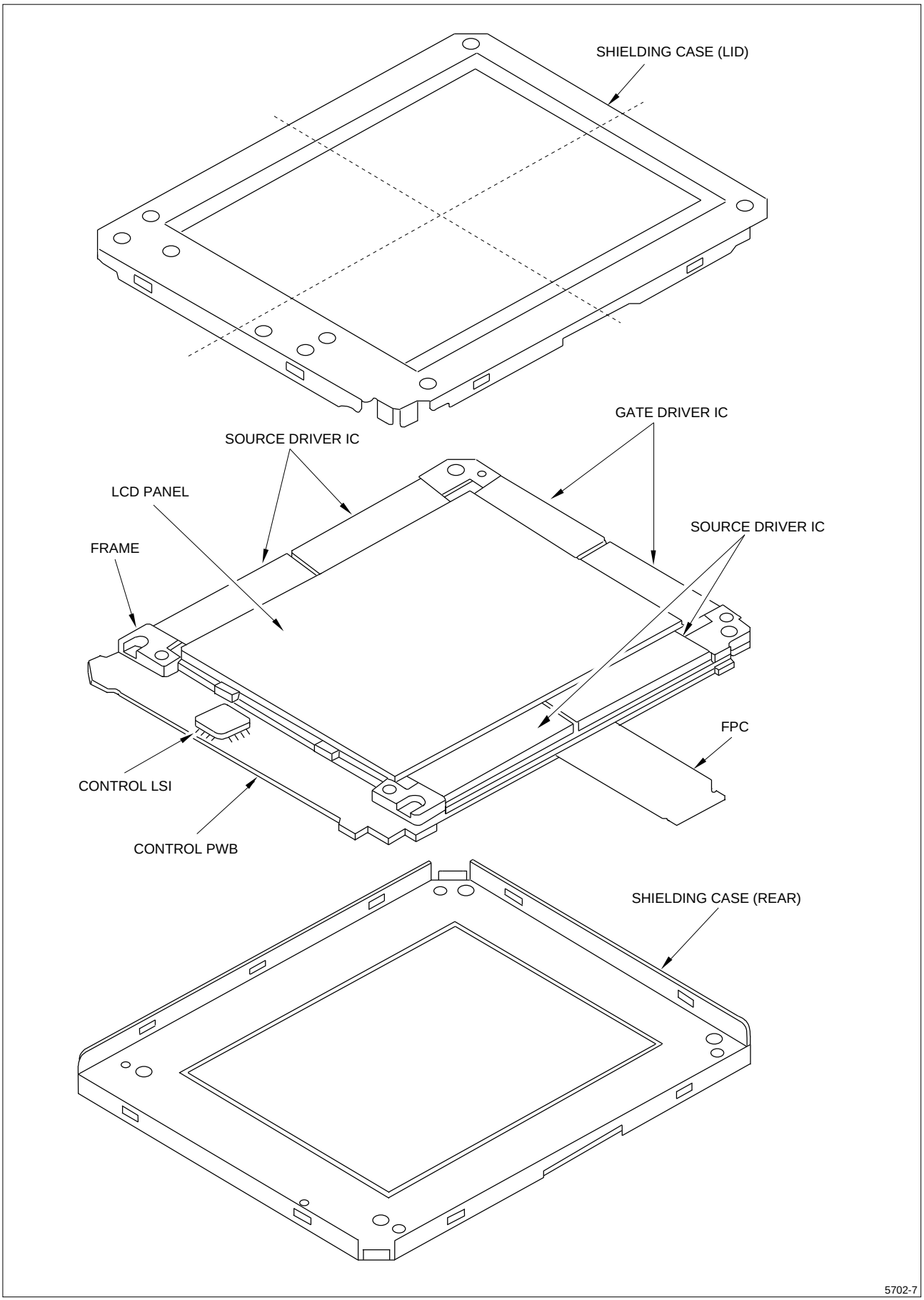



**Figure 2. LQ4RE01/LQ4RE02 TFT-LCD Module Construction**

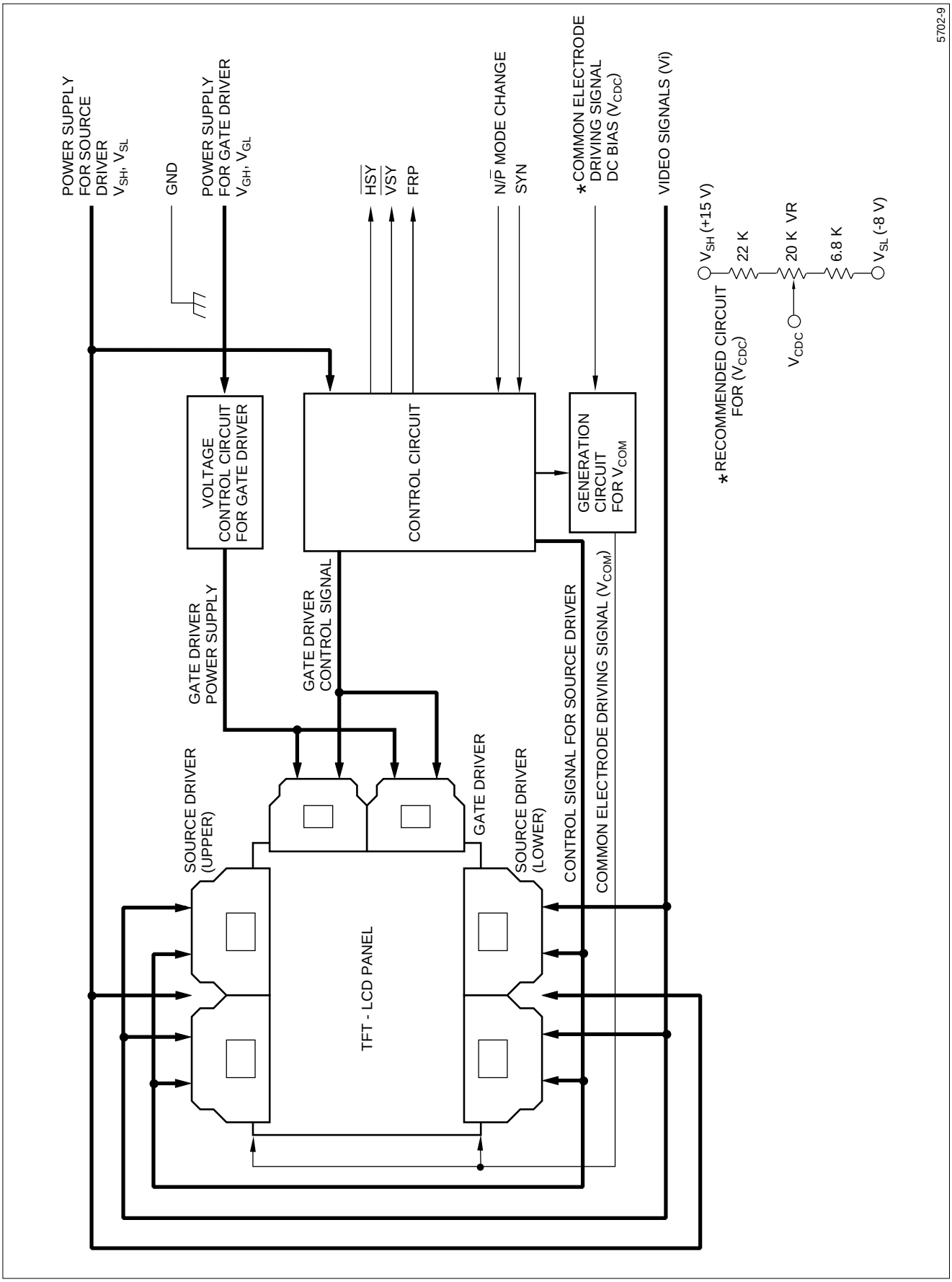



**Figure 3. LQ4RE01/LQ4RE02 Block Diagram**

## MECHANICAL SPECIFICATIONS

| PARAMETER | SPECIFICATIONS | UNIT | NOTE |
|---|---|---|---|
| Display Format | 37,440 | pixels | – |
| | 479 (W) × 234 (H) | dots | – |
| Active Area | 81.9 (W) × 61.8 (H) | mm | – |
| Screen Size (Diagonal) | 10 (4") | cm | – |
| Pixel Pitch | 0.171 (W) × 0.264 (H) | mm | – |
| Pixel Configuration | RGB Delta Configuration | – | – |
| Outline Dimensions | 122 (W) × 100 (H) × 6.6 (D) | mm | 1 |
| Weight | 135 ±10 | g | – |

**NOTE:**

1. Excludes protrusions.

## ABSOLUTE MAXIMUM RATINGS (GND = 0 V, $t_A$ = 25°C)

| SYMBOL | PARAMETER | | MIN. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|
| $V_{SH}$ | Supply Voltage for Source Driver | 'H' Level | –0.3 | +6.0 | V | – |
| $V_{SL}$ | | 'L' Level | –12 | +0.3 | V | – |
| $V_{GH}$ | Supply Voltage for Gate Driver | 'H' Level | –0.3 | +15 | V | – |
| $V_{GL}$ | | 'L' Level | –23 | +0.3 | V | – |
| Vi | Analog Input Signal | | $V_{SL}$ – 0.3 | $V_{SH}$ +0.3 | V | 1 |
| $V_I$ | Digital Input/Output Signal | | –0.3 | $V_{SH}$ +0.3 | V | 2 |
| $V_{CDC}$ | Common Electrode Driving Signal DC Bias Voltage | | –11 | –1 | V | – |
| Tstg | Storage Temperature | | –25 | 60 | °C | 3 |
| Topp | Operating Temperature | | 0 | 50 | °C | 3, 4 |

**NOTES:**

Evaluation of display quality shall be done under the normal operation state (25°C).

1. VR, VG, VB, terminals (Video signal).
2. $\overline{HSY}$, FRP, SYN, $\overline{VSY}$, N/$\overline{P}$ terminals.
3. No dew condensation. In case of dew condensation, it is possible to cause electrical leaks, so the specifications described here may not be satisfied.
4. Panel temperature.

## INPUT/OUTPUT TERMINALS

| PIN NUMBER | SYMBOL | I/O | DESCRIPTION | NOTE |
|---|---|---|---|---|
| 1 | $\overline{HSY}$ | O | Internal Horizontal Sync Signal (In phase with SYN) | – |
| 2 | FRP | O | Polarity Alternating Signal for Video | – |
| 3 | SYN | I | Composite Sync Signal | – |
| 4 | $V_{GH}$ | I | Power Supply for Gate Driver (‘H’ Level) | – |
| 5 | $V_{GL}$ | I | Power Supply for Gate Driver (‘L’ Level) | – |
| 6 | VB | I | Video Signal (Blue) | – |
| 7 | VR | I | Video Signal (Red) | – |
| 8 | VG | I | Video Signal (Green) | – |
| 9 | GND | I | Ground | – |
| 10 | $V_{SH}$ | I | Power Supply for Source Driver (‘H’ Level) | – |
| 11 | $V_{SL}$ | I | Power Supply for Source Driver (‘L’ Level) | – |
| 12 | $V_{CDC}$ | I | Common Electrode Driving Signal DC Bias | 1 |
| 13 | N/$\overline{P}$ | I | Mode Change Terminal (NTSC (M) = $V_{SH}$/PAL (BG) = GND) | – |
| 14 | $\overline{VSY}$ | O | Internal Vertical Sync Signal (In phase with SYN) | – |
| 15 | TST | – | This is Electrically Opened During Operation | – |
| 16 | | | | |

**NOTES:**

1. Could be kept electrically open during operation. In this case, variable resistor $V_{CDC}$ must be adjusted to get the highest contrast ratio.

***CAUTION:*** Shielding case that is separated from GND terminal is electrically opened.

## RECOMMENDED OPERATING CONDITIONS (GND = 0 V, $t_A$ = 25°C)

| SYMBOL | PARAMETER | | MIN. | TYP. | MAX. | UNIT | CONDITION | NOTE |
|---|---|---|---|---|---|---|---|---|
| $V_{SH}$ | Supply Voltage for Source Driver | 'H' Level | +4.8 | +5.0 | +5.2 | V | – | – |
| $V_{SL}$ | | 'L' Level | –7.6 | –8.0 | –8.4 | V | – | – |
| $V_{GH}$ | Supply Voltage for Gate Driver | 'H' Level | +12.5 | +13 | +13.5 | V | – | – |
| $V_{GL}$ | | 'L' Level | –19 | –20 | –21 | V | – | – |
| $V_{iAC}$ | Analog Input Voltage | | ±2.5 | – | ±3.4 | V | AC Component | 1, 2 |
| $V_{iDC}$ | | | $V_{SM}$ –0.2 | $V_{SM}$ | $V_{SM}$ +0.2 | V | DC Component | 1, 3 |
| $V_{IH}$ | Digital Input Voltage | 'H' Level | +3.5 | – | $V_{SH}$ | V | – | 4, 5 |
| $V_{IL}$ | | 'L' Level | 0 | – | +1.5 | V | | |
| $V_{OH}$ | Digital Output Voltage | 'H' Level | +3.5 | – | $V_{SH}$ | V | – | 6 |
| $V_{OL}$ | | 'L' Level | 0 | – | +1.5 | V | | |
| $V_{CDC}$ | Common Electrode Driving Signal DC Bias Voltage | | –1.5 | –3.0 | –6.5 | V | DC Component | 7 |

**NOTES:**

The block diagram is shown in Figure 3.

***CAUTION:*** Turn on or off the power supply in the following order:

ON . . . $V_{SH} \rightarrow V_{GH} \rightarrow V_{GL} \rightarrow V_{SL}$

OFF . . . $V_{SL} \rightarrow V_{GL} \rightarrow V_{GH} \rightarrow V_{SH}$

Be sure to supply all power voltages before inputting input signals.

1. VR, VG, VB terminal (Video signal). Input capacitance: 200 pF (TYP).
2. Positive and negative waveforms should have the same amplitude.
3. $V_{SM} = \frac{(V_{SH} - V_{SL})}{2}$.
4. Input capacitance: 15 pF (TYP).
5. SYN, N/$\overline{P}$ terminal.
6. $\overline{HSY}$, $\overline{VSY}$, FRP terminal (load resistance = 20 kΩ).
7. Adjusted for each module so as to attain maximum contrast ratio. Refer to 'Adjustment Method for Optimum DC Bias' for adjusting.

## CURRENT DISSIPATION ($t_A$ = 25°C)

| SYMBOL | PARAMETER | | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{SH}$ | Current for Source Driver | 'H' Level | $V_{SH}$ = +5 V | – | +50 | +75 | mA |
| $I_{SL}$ | | 'L' Level | $V_{SL}$ = –8 V | – | –35 | –55 | mA |
| $I_{GH}$ | Current for Gate Driver | 'H' Level | $V_{GH}$ = +13 V | – | +2 | +3 | mA |
| $I_{GL}$ | | 'L' Level | $V_{GL}$ = –20 V | – | –2 | –3 | mA |

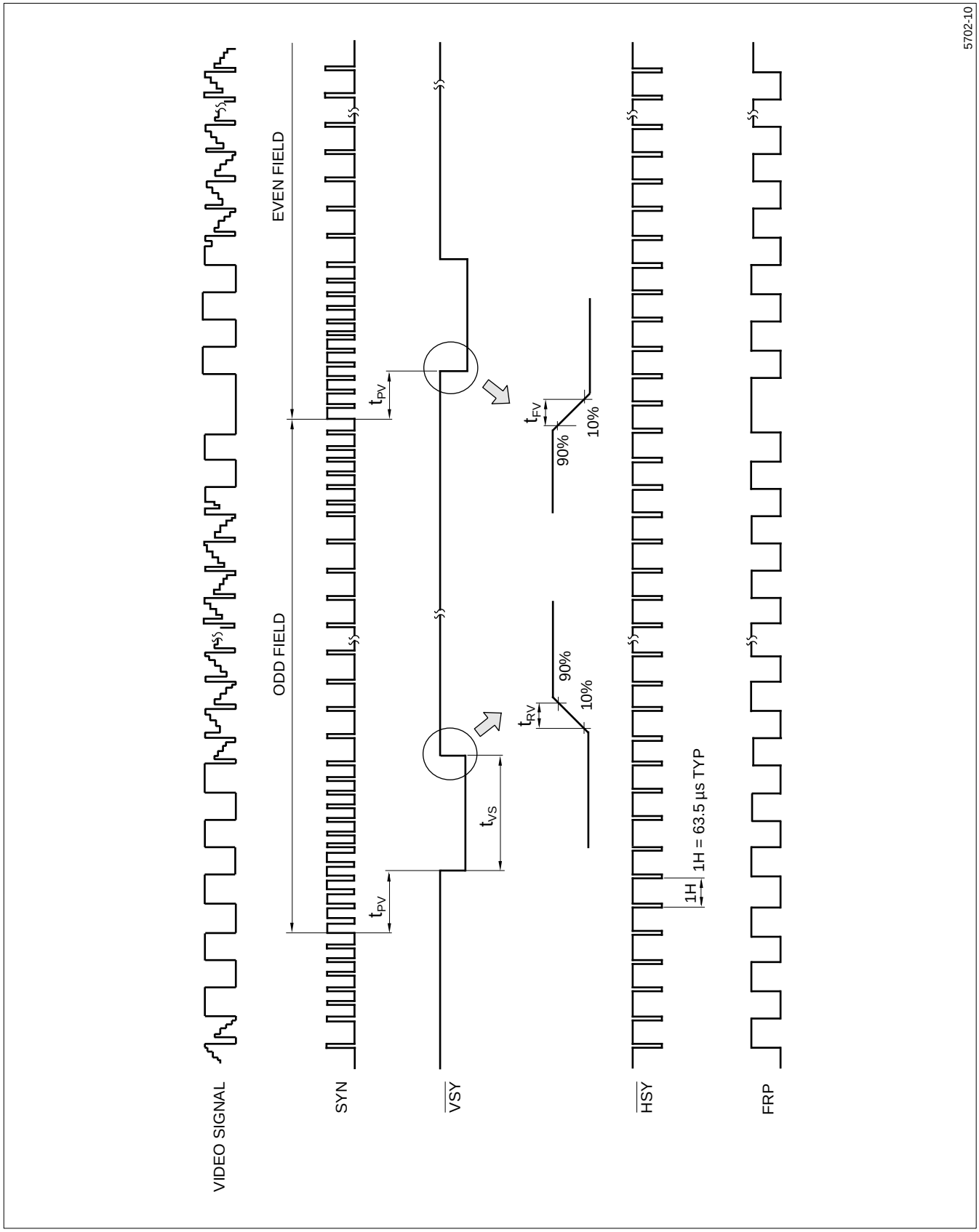



**Figure 4a. Input/Output Signal Waveforms (NTSC)**

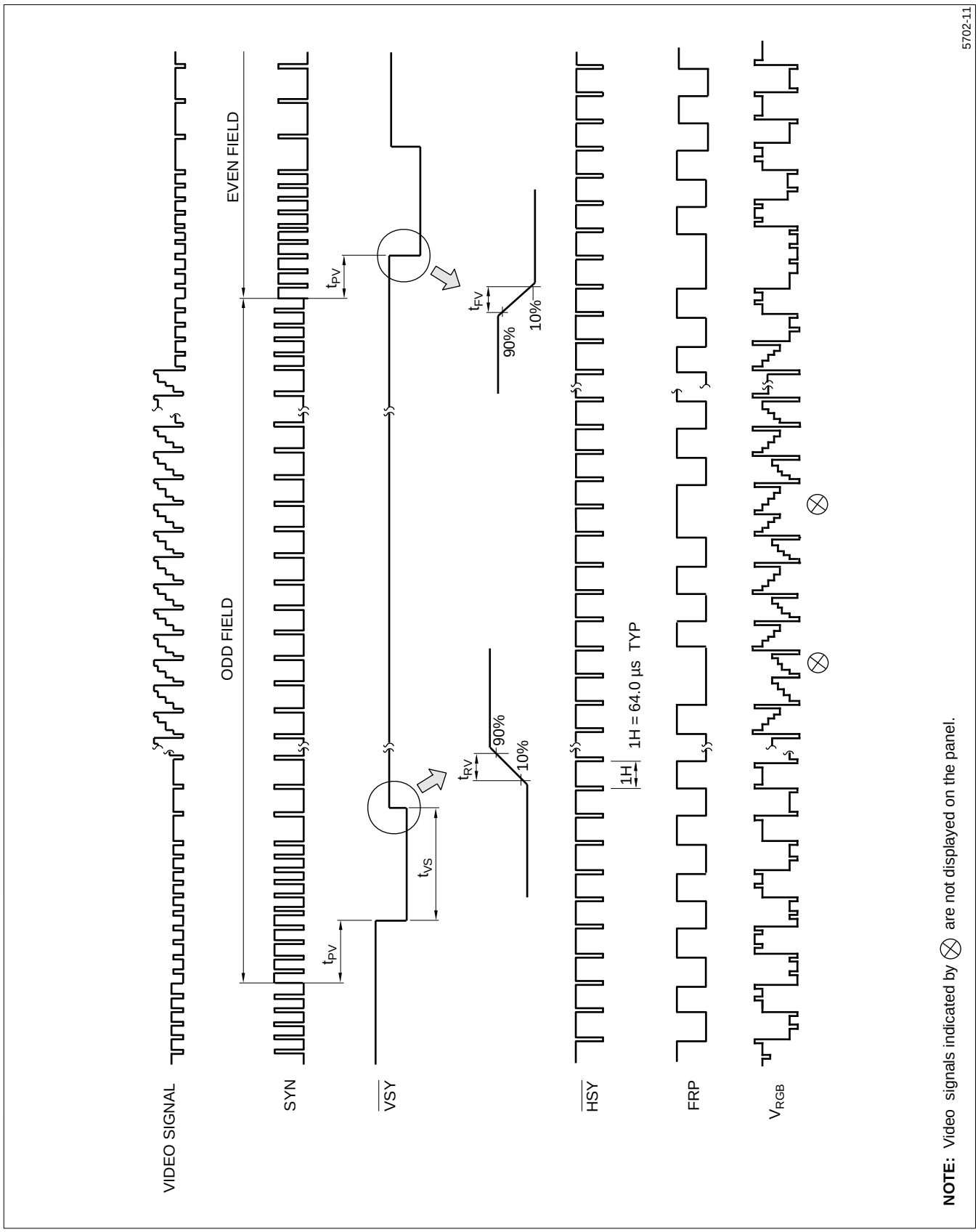



**Figure 4b. Input/Output Signal Waveforms (PAL)**

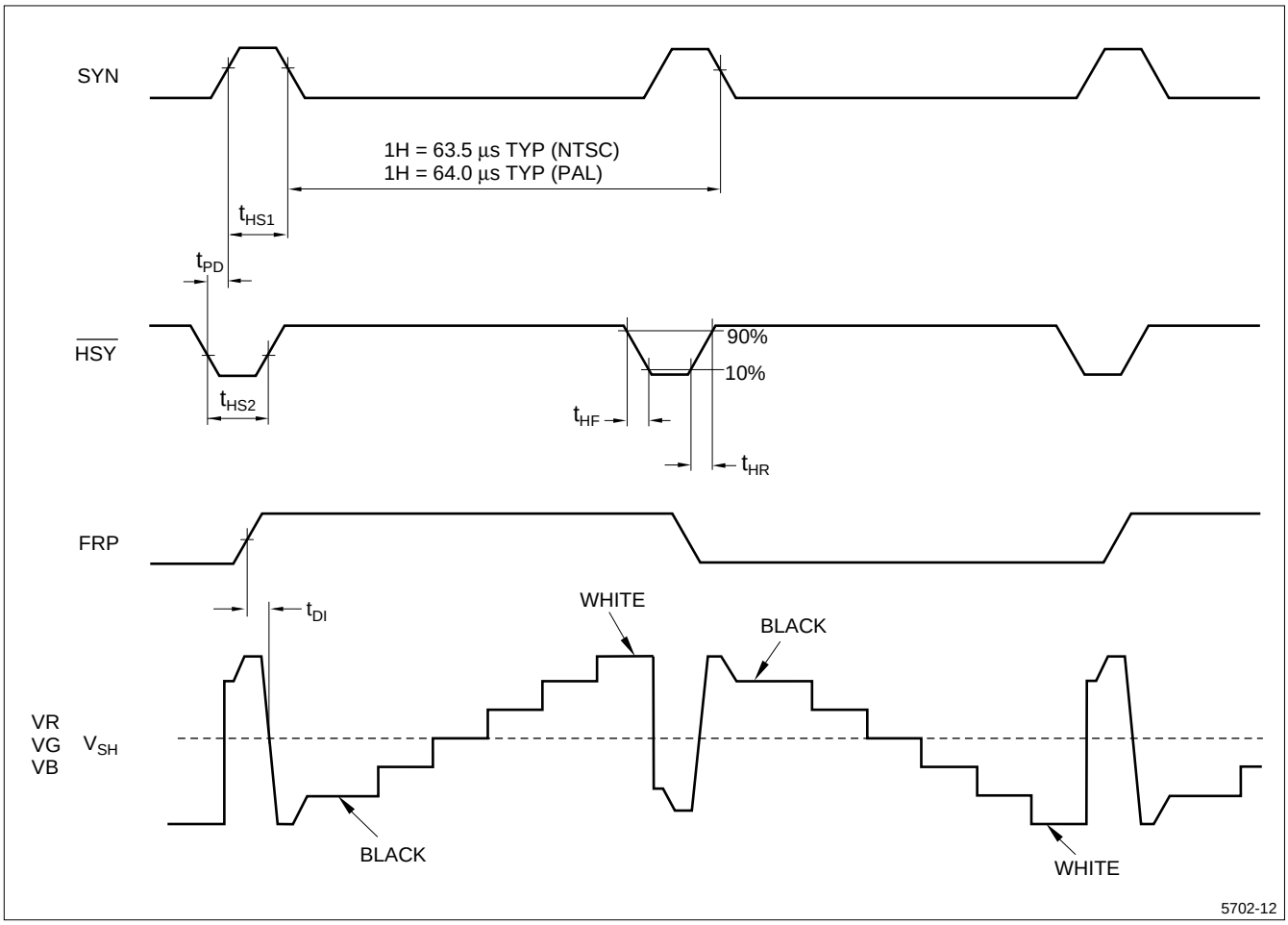



**Figure 5. Input/Output Signal Timing Chart**

## TIMING CHARACTERISTICS – INPUT/OUTPUT SIGNALS
## ($V_{SH}$ = + 5.0 V, $V_{SL}$ = –8.0 V) ($V_{GH}$ = +13.0 V, $V_{GL}$ = –20.0 V)

### (NTSC (M): $f_H$ = 15.7 kHz, $f_V$ = 60 Hz) (PAL (B, G): $f_H$ = 15.6 kHz, $f_V$ = 50 Hz)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|
| $t_{HSI}$ | Horizontal Sync – Input Pulse Width | 4.2 | 4.7 | 5.7 | µs | – |
| $t_{HS2}$ | Horizontal Sync – Output Pulse Width | 2.3 | 4.7 | 7.1 | | $f = f_H$ |
| $f_{COM}$ | Polarity Alternating Signal – Frequency | – | $f_H$ / 2 | – | Hz | – |
| $t_{D1}$ | Polarity Alternating Signal – Delay Time | 0 | 2.0 | 4.0 | µs | – |
| $t_{PD}$ | Horizontal Sync Phase Difference | 0.6 | 2 | 3.4 | | 1 |
| $t_{VS}$ | Vertical Sync Output Pulse Width | 243 | 256 | 269 | | $4/f_H$ |
| $t_{PV}$ | Vertical Sync Phase Difference | 121/90 | 127/95 | 133/100 | | 2 |
| $t_{RH}$ | Horizontal Sync – Signal Rising Time | – | – | 0.3 | | 3 |
| $t_{FH}$ | Horizontal Sync – Signal Falling Time | – | – | 0.4 | | |
| $t_{RV}$ | Vertical Sync – Signal Rising Time | – | – | 3 | | |
| $t_{FV}$ | Vertical Sync – Signal Falling Time | – | | 3 | | |

**NOTES:**

1. Positive when $\overline{HSY}$ proceeds SYN (Reference: adjusted value PAL/1.3 ± 0.7 µs).
2. Odd field/Even field ($2/f_H$ / $1.5/f_H$).
3. Load capacitance at measurement circuit. $C_L$ = 10 pF.

### Display Time Range

When sync signal of NTSC (M) system is applied:

- Horizontally: 12.5 µs to 62.4 µs from the falling edge of $\overline{HSY}$.
- Vertically: 19H to 252H from the falling edge of $\overline{VSY}$.

When sync signal of PAL (B, G) system is applied:

- Horizontally: 12.9 µs to 63.3 µs from the falling edge of $\overline{HSY}$.
- Vertically: 25H to 297H from the falling edge of $\overline{VSY}$

The signal of (14n + 11)H, (14n + 19)H/Even field, (14n + 16)H (14n +22)H/Odd field (n = 1, 2, 3 . . .) are not displayed on the panel.

## OPTICAL CHARACTERISTICS – BACKLIGHT ($t_A$ = 25°C)

Brightness: Less than 3500 cd/m$^2$.
Wavelength: Component shorter than 400 nm must be cut off.

| SYMBOL | PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|---|
| $\Delta\theta$ 11 | Viewing Angle Range | CR ≥10 | 30 (10) | – | – | degrees | LQ4RE01 (LQ4RE02) 1, 2 |
| $\Delta\theta$ 12 | | | 10 (30) | – | – | | |
| $\Delta\theta$ 2 | | | 45 | – | – | | |
| $CR_{MAX}$ | Contrast Ratio | $\theta$ = 0° | 30 | – | – | – | 2, 3 |
| $t_R$ | Response Time – Rise | $\theta$ = 15° | – | 30 | – | ms | 2, 4 |
| $t_D$ | Response Time – Decay | | – | 50 | – | ms | |
| Tr | Transmission | $\theta$ = 0° | 2.4 | – | – | % | 5 |
| $\Delta$x | Chromaticity Shift | – | –0.01 | – | +0.03 | – | 6 |
| $\Delta$y | | – | –0.005 | | +0.035 | – | |

**NOTES:**

1. Viewing angle range is defined in Figure 6.
2. Applied voltage conditions:
   a. $V_{CDC}$ is adjusted so as to attain maximum contrast ratio.
   b. White Vi = $Vi_{50}$ ±1.5 V
      Black Vi = $Vi_{50}$ ±2.0 V
      $Vi_{50}$: The analog input voltage when transmission is 50%. Transmission 100% is defined as the panel transmission with all the input terminals of module electrically open.
3. Contrast ratio is defined as follows:

$$\text{Contrast ratio} = \frac{\text{Photodetector output with LCD being 'white'}}{\text{Photodetector output with LCD being 'black'}}$$

4. Response time is obtained by measuring the transition time of photodetector output, when input signals are applied to make the area 'black' to and from 'white' (see Figure 7).
5. Transmission is defined as follows:

$$\text{Transmission} = \frac{\text{Photodetector output voltage when measuring the brightness of the LCD panel placed on the light source with no applied voltage}}{\text{Photodetector output voltage when measuring the light source brightness}} \quad (\theta = 0°)$$

6. Chromacity shift is the difference between the light source and the panel placed on it.
   The light source chromacity should be (x = 0.320, y = 0.340).

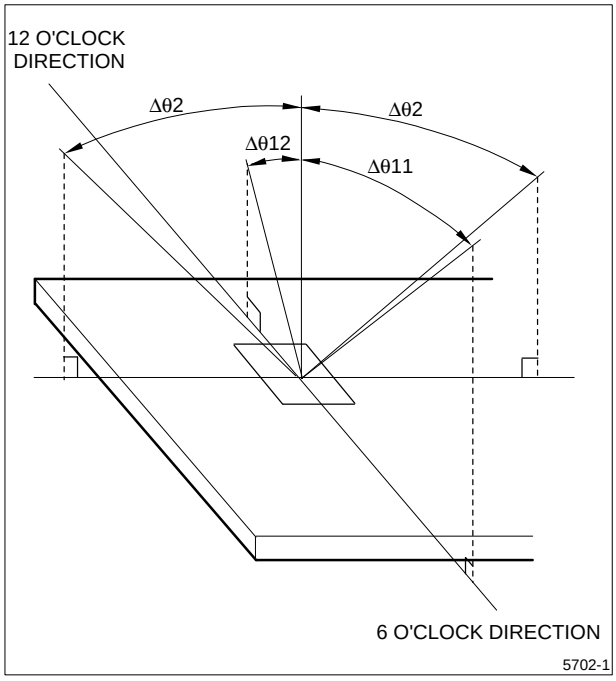



**Figure 6. Definition of Viewing Angle**

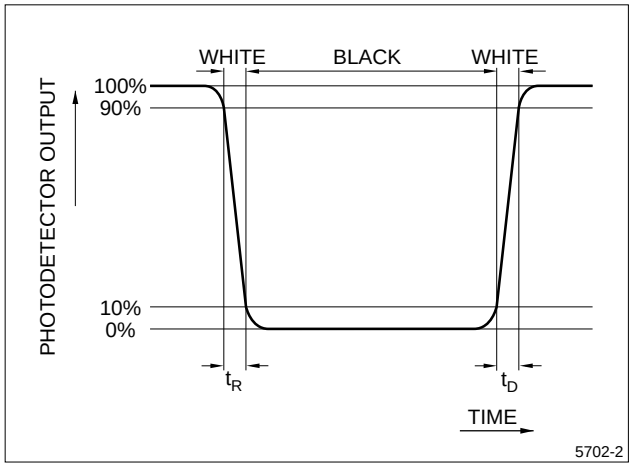



**Figure 7. Definition of Response Time**

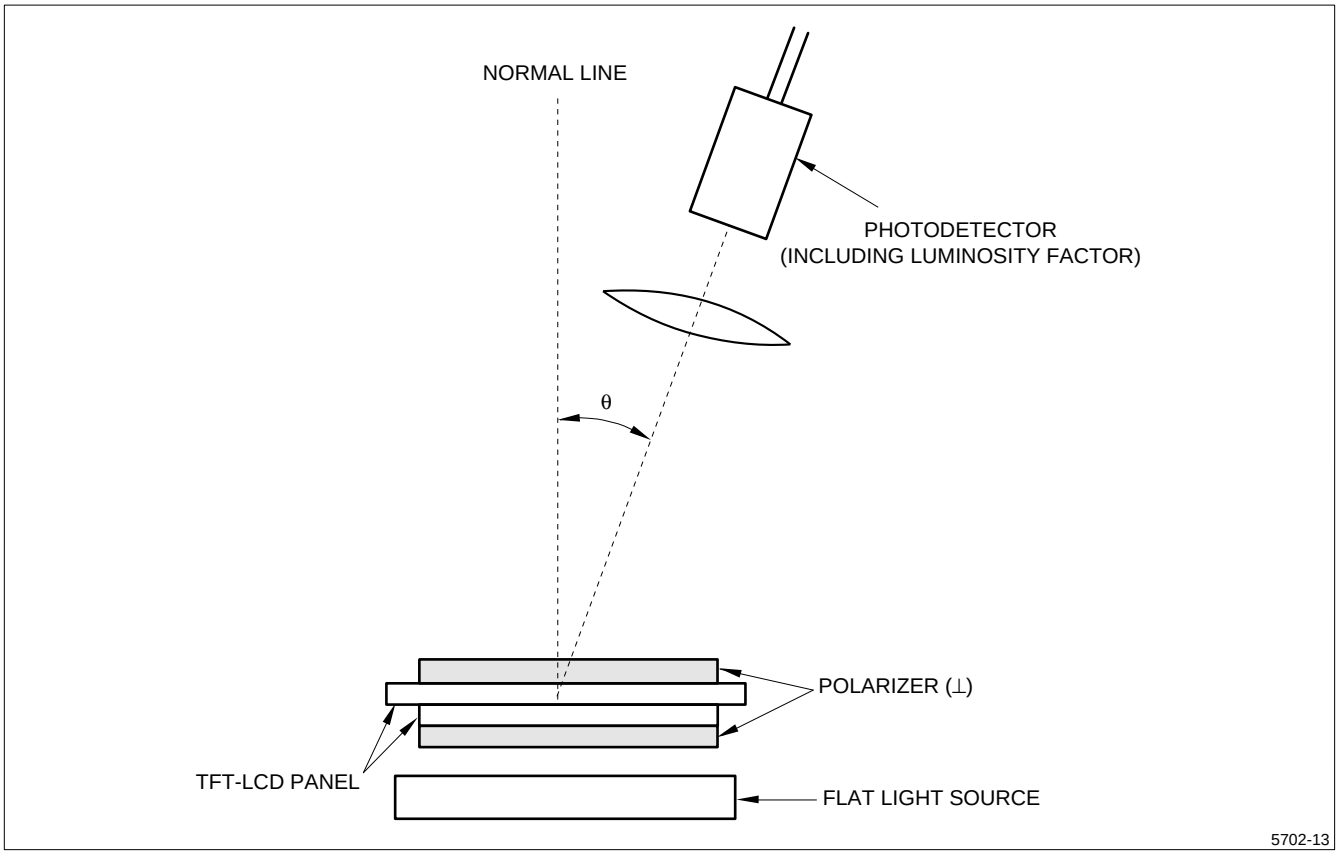



**Figure 8. Optical Characteristics Measuring Method**

## MECHANICAL CHARACTERISTICS

### External Appearance

There shall not be any conspicuous defects. (See Outline Dimensions diagram.)

### FPC Bending Test

In the tests shown in Figures 9 and 10, no open lines happen before the following cycles:

- Figure 9: MIT test – 500 cycles
- Figure 10: IPC test – 100,000 cycles

### Panel Durability

The panel shall not break when the panel center is pressed with a 2 kg force by a 15 mm diameter smooth, flat surface.

***CAUTION:*** The least force can cause malfunction if it is applied on the active area for prolonged periods.

### Maximum Resin Region

As shown in Figure 11, resin may fill up to the same level as a line connecting the upper ridges of a panel and a shielding case.

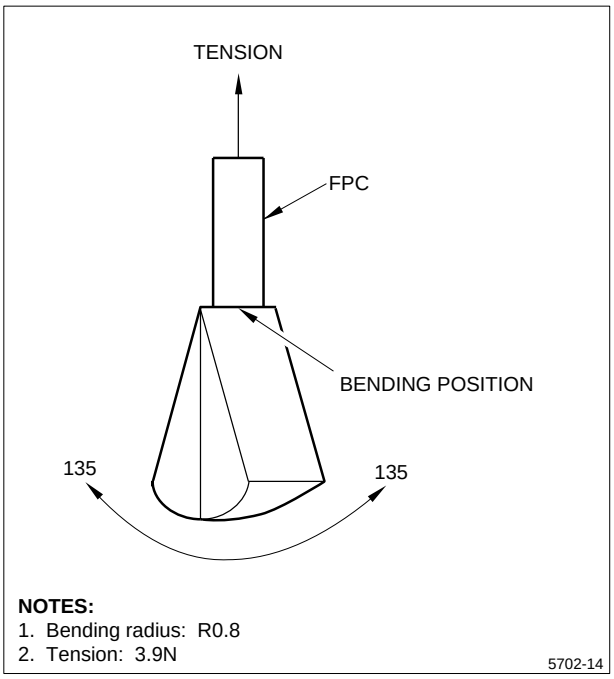



**Figure 9. MIT Test (JIS P8115)**

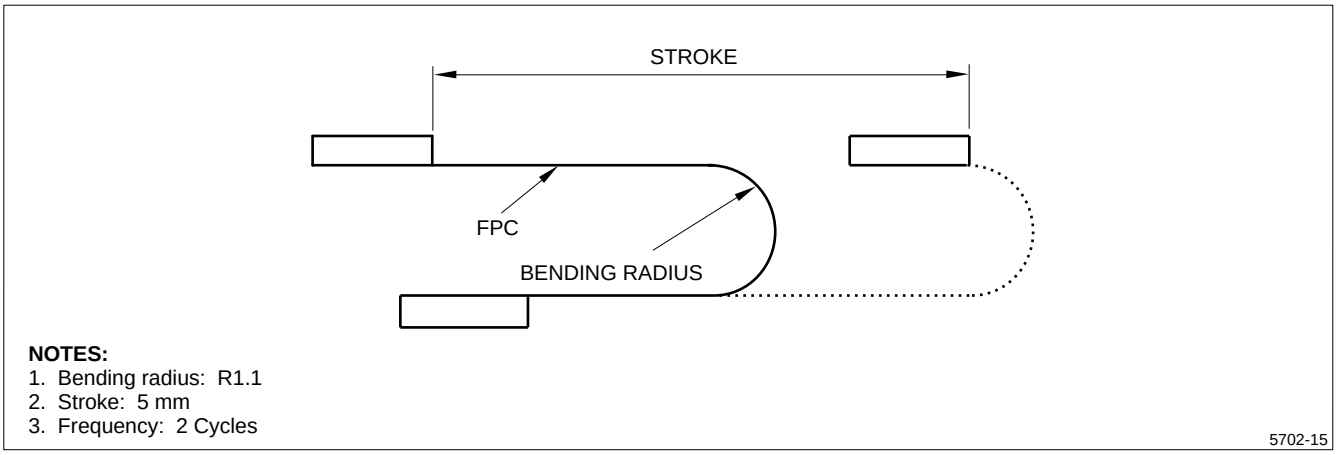



**Figure 10. IPC Test**

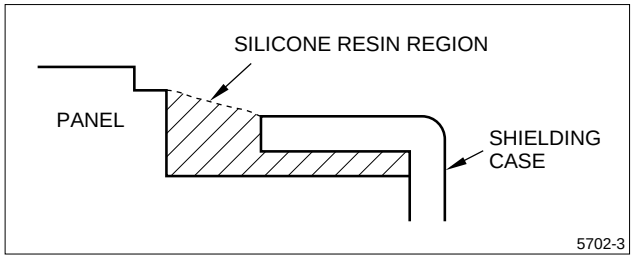



**Figure 11. Maximum Resin Region**

## DISPLAY QUALITY

The rejection criteria for display quality of color TFT-LCD modules are specified in Incoming Inspection Standard.

## HANDLING INSTRUCTIONS

### Mounting of Module

- This module is designed to be mounted on equipment using the mounting tabs in the four corners of the module. When installing the module, handle carefully to avoid undue stress, such as twising or bending.
- The module should be affixed to the metal part of equipment. Contact with the resin region may cause damage.

### Precautions in Mounting

- The polarizer, which is made of soft material and susceptible to flaws, must be handled carefully. Protective film laminator is applied on the surface to protect it against scratches and dirt. Peel off the laminator just before using to avoid static electricity.

### Precautions When Peeling Off Laminator

*Working Environment*

When the laminator is peeled off, static electricity may cause dust to stick to the polarizer surface. To avoid this, the following working environment is desirable:

- Floor: Conductive treatment of 1 MΩ or more on the tile or a conductive mat or conductive paint on the tile.
- Clean, dust-free room with an adhesive mat placed in the doorway.
- Humidity: 50% to 70% RH.
- Temperature: 15° to 27°C.
- Workers shall wear conductive shoes, work clothes, gloves, and a ground strap.

*Working Procedures*

- Direct the wind of the heated ionized air discharging blower somewhat downward to ensure that the module is blown sufficiently. Keep the distance between the module and the blower within 20 cm (see Figure 12a).
- Attach adhesive tape to the laminater part near the discharging blower to protect polarizer against flaws (see Figure 12b).
- Peel off laminator, pulling adhesive tape slowly to your side taking five or more seconds. It is important that it takes more than five seconds.
- After peeling off the laminator, pass the module to the next work process immediately without getting the module dusty.

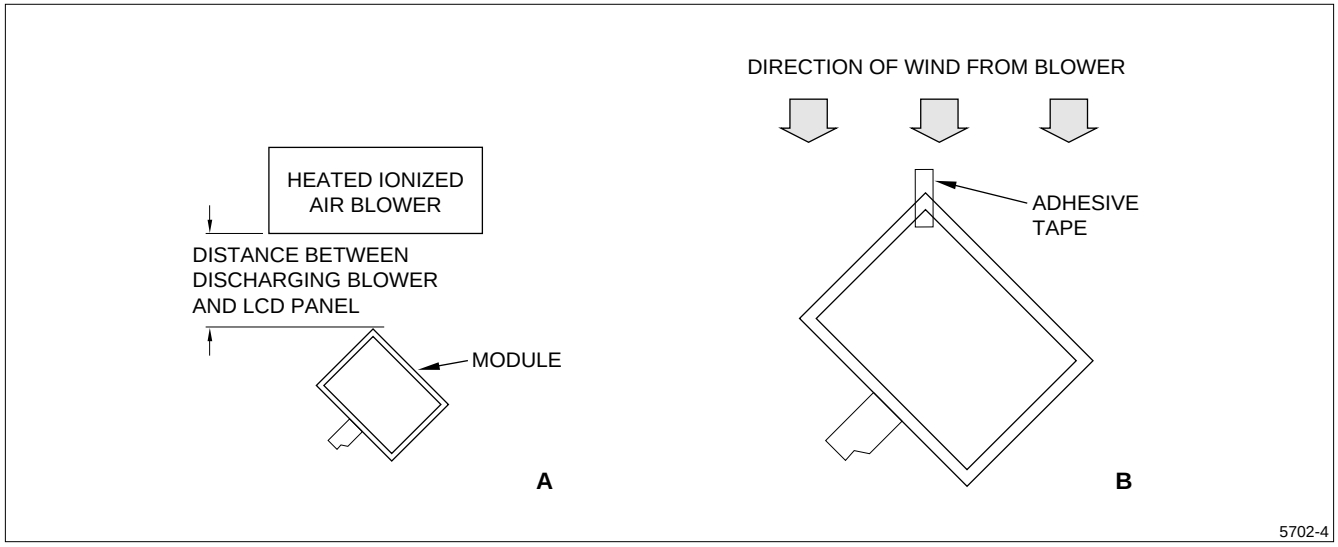



**Figure 12. Proper Use of Discharging Blower**

- Methods of removing dust from polarizer:
  - Blow off dust with $N_2$ blower for which static electricity preventive measures have been taken. An ionized air gun (Hugle Electronics Co.) is recommended.
  - Since the polarizer is easily damaged, avoid wiping it. If this is unavoidable, wipe it carefully with a lens cleaning cloth, breathing on it. 'Belleseime' (Kanebo, Ltd.) is desirable.
- When metal parts of the module (shielding lid and rear case) are soiled, wipe them with a soft, dry cloth. For stubborn dirt, wipe the part, breathing gently on it.
- Wipe off liquid immediately since it can cause color changes and staining.
- The TFT-LCD module is made of glass plates. Use care when handling it to avoid breakage.
- This unit contains CMOS LSIs which are sensitive to electrostatic charges. Use care to protect the unit from electrostatic discharges.

### Precautions in Adjusting Module

- Adjusting volumes (H-HOLD, $V_{CO}$) on the module have been set optimally before shipment. If adjusted values are changed, the specifications described in this technical literature may not be satisfied.

### Other Precautions

- Do not expose the unit to direct sunlight, strong ultraviolet light, etc., for prolonged periods.
- Store the unit at normal room temperature to prevent the LC from converting to liquid (due to excessive temperature changes).
- If the LCD panel breaks, the liquid crystal may escape from the panel. Since the liquid crystal is harmful, do not put it into the eyes or mouth. When liquid crystal sticks to hands, feet or clothes, wash it out immediately with soap.
- Static image should not be displayed for more than five minutes in order to prevent occurrence of residual image. It is recommended that display pattern be changed periodically or operation of display ON/OFF should be turned intermittently.
- $V_{CDC}$ must be adjusted according to 'Adjusting Method of Optimum Common Electrode DC Bias Voltage.' No adjustment causes the deterioration of display quality.
- Observe all other precautionary requirements in handling general electronic components.

## SHIPPING REQUIREMENTS

The packing form is shown in Figure 13.

### Carton Storage Conditions

- Number of layers of cartons in pile: 12 layers maximum.
- Environmental conditions:
  - Temperature: 0°C to 40°C.
  - Humidity: 60% RH or less (at 40°C). No dew condensation at low temperatures and high humidity.
  - Atmosphere: Harmful gases such as acid and alkali which corrode electronic components and/or wires must not be detected.
  - Storage Period: Approximately three months.
  - Opening of Package: To prevent the LCD module from being damaged by static electricity, adjust the room humidity to 50% RH or higher and provide an appropriate measure for electostatic grounding before opening the package.

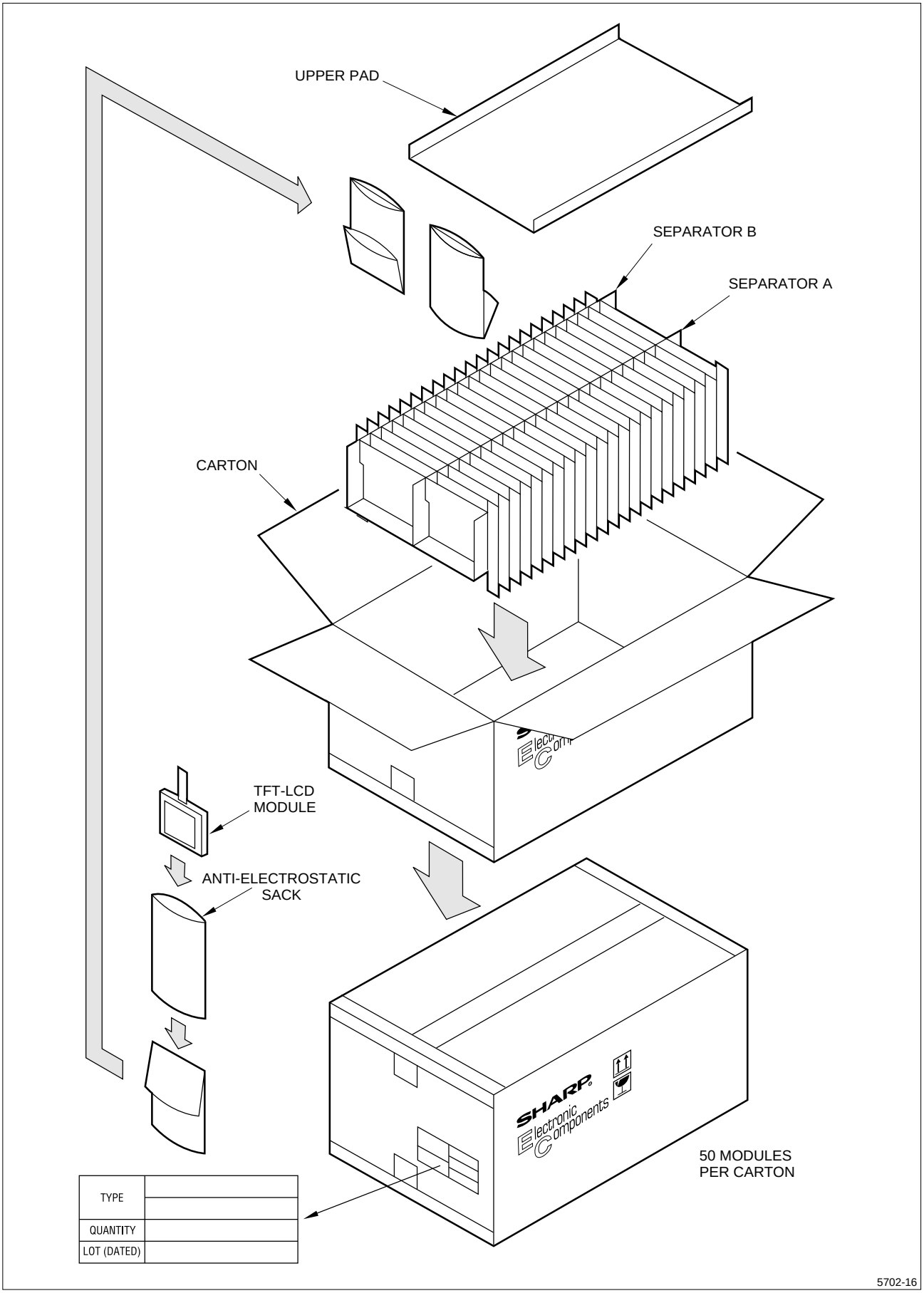



**Figure 13. Packing Form**

## RELIABILITY TEST ITEMS

| NUMBER | TEST ITEM | CONDITIONS |
|---|---|---|
| 1 | High-Temperature Storage Test | $t_P$ = +60°C, 240 H |
| 2 | Low-Temperature Storage Test | $t_P$ = –25°C, 240 H |
| 3 | High-Temperature and High-Humidity Operating Test | $t_P$ = +40°C, 95% RH, 240 H |
| 4 | High-Temperature Operating Test | $t_P$ = +50°C, 240 H |
| 5 | Low-Temperature Operating Test | $t_P$ = 0°C, 240 H |
| 6 | Electrostatic Discharge Test | ±200 V, 200 pF (0 Ω), Once for each terminal |
| 7 | Shock Test | 980 m/s$^2$, 6 ms, ±X, ±Y, ±Z, three times for each direction (JIS C7021, A-7 Condition C) |
| 8 | Vibration Test | Frequency range: 10 Hz to 55 Hz<br>Stroke: 1.5 mm<br>Sweep: 10 Hz to 55 Hz to 10 Hz<br>Two hours for each direction of X/Y/Z (six hours total)<br>(JIS C7021, A-10 Condition A) |
| 9 | Heat Shock Test | –25°C to –60°C/5 cycles<br>(1 H) (1 H) |

### Result Evaluation Criteria

Under the display quality test conditions with normal operation state, there shall be no change which may affect practical display function.

## OTHER INFORMATION

If any problem should arise from this specification, the supplier and the user should work out a mutually acceptable solution.

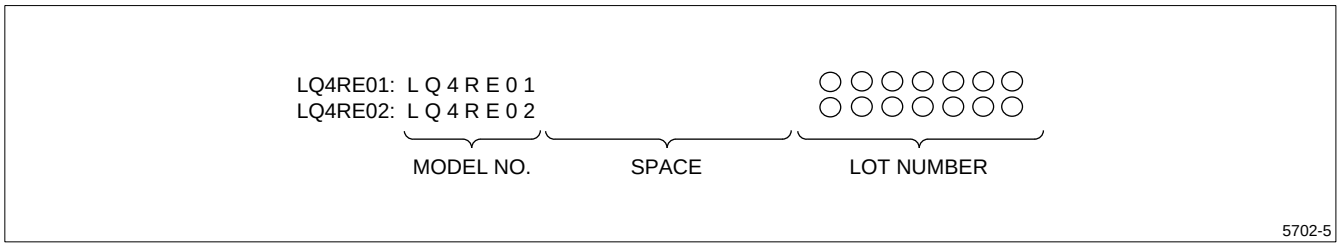



**Figure 14. Lot Number Label**

## CONSTRUCTION OF TFT-LCD MODULE

This LCD module is composed of a Si-TFT-LCD panel, driving ICs for the LCD panel, and a control circuit for the driver ICs.

The driver ICs are divided into two types: a source driver (data driver) which receives RGB signals and sends them sequentially by one horizontal line of the LCD panel, and a gate driver (scan driver) which scans 234 gate lines of the LCD panel.

The circuit diagram is shown in Figure 3.

This module receives power supplies (for source driver: $V_S$, for gate driver $V_G$, RGB video signals, common electrode driving signal DC bias ($V_{CDC}$), and a composite synchronizing signal (SYN), and then it displays a picture on the LCD panel.

The control circuit receives the composite synchronizing signal separated in the video interface circuit, generates clock pulses (phase-locked to the horizontal synchronizing pulse in the SYN) synchronized with the composite synchronizing signal and gate and source drivers-driving signals. It outputs internal horizontal synchronizing signal ($\overline{HSY}$), internal vertical synchronizing signal ($\overline{VSY}$), and polarity alternating signal (FRP).

$\overline{VSY}$, $\overline{HSY}$, for example, may be used to display characters on the screen when this module is applied to a TV set. FRP is used to alternate the polarity of the RGB video signals.

Power supplies to this module are 5 V ($V_{SH}$), 0 V (GND), –8 V ($V_{SL}$), 13 V ($V_{GH}$) and –20 V ($V_{GL}$). Control LSI operates on 0 V to 5 V line so that it outputs SYN, FRP, $\overline{HSY}$ and $\overline{VSY}$ at 0 V to 5 V level.

Power supplies to the video signal polarity alternating circuit (which is not included in this LCD module, but is necessary to alternate the polarity of the RGB video signals) should be $V_{SH}$ and $V_{SL}$.

## EXAMPLE OF TFT-LCD TV

Figure 15 shows a block diagram example of the TFT-LCD module applied to a TV set.

The block encircled by the dotted line is this TFT-LCD module. The block encircled by a double dotted line is the special signal-processing blocks used to drive the TFT-LCD module. Other signal processing parts are the same as those in ordinary CRT-TVs.

The following signals must be supplied to this module from the exterior:

- Composite synchronizing signal: SYN
- RGB video signals
- Common electrode driving signal DC bias: $V_{CDC}$

The following signals are output from this module to the exterior:

- Polarity alternating signal: FRP
- Internal horizontal synchronized signal: $\overline{HSY}$
- Internal vertical synchronized signal: $\overline{VSY}$

The composite synchronizing signal is used to write a video signal on each LCD pixel correctly. RGB video signals, (which must be supplied from external circuit) are finally lead to the liquid-crystal layer of each pixel by way of source-driver IC and TFT. The dynamic range of the signals is 5 $V_{P-P}$ from black level to white level. In order to prevent liquid crystal from electro-chemical degradation, polarity of the video signals must be alternated. Output signal FRP should be used to alternate the polarity of the video signals.

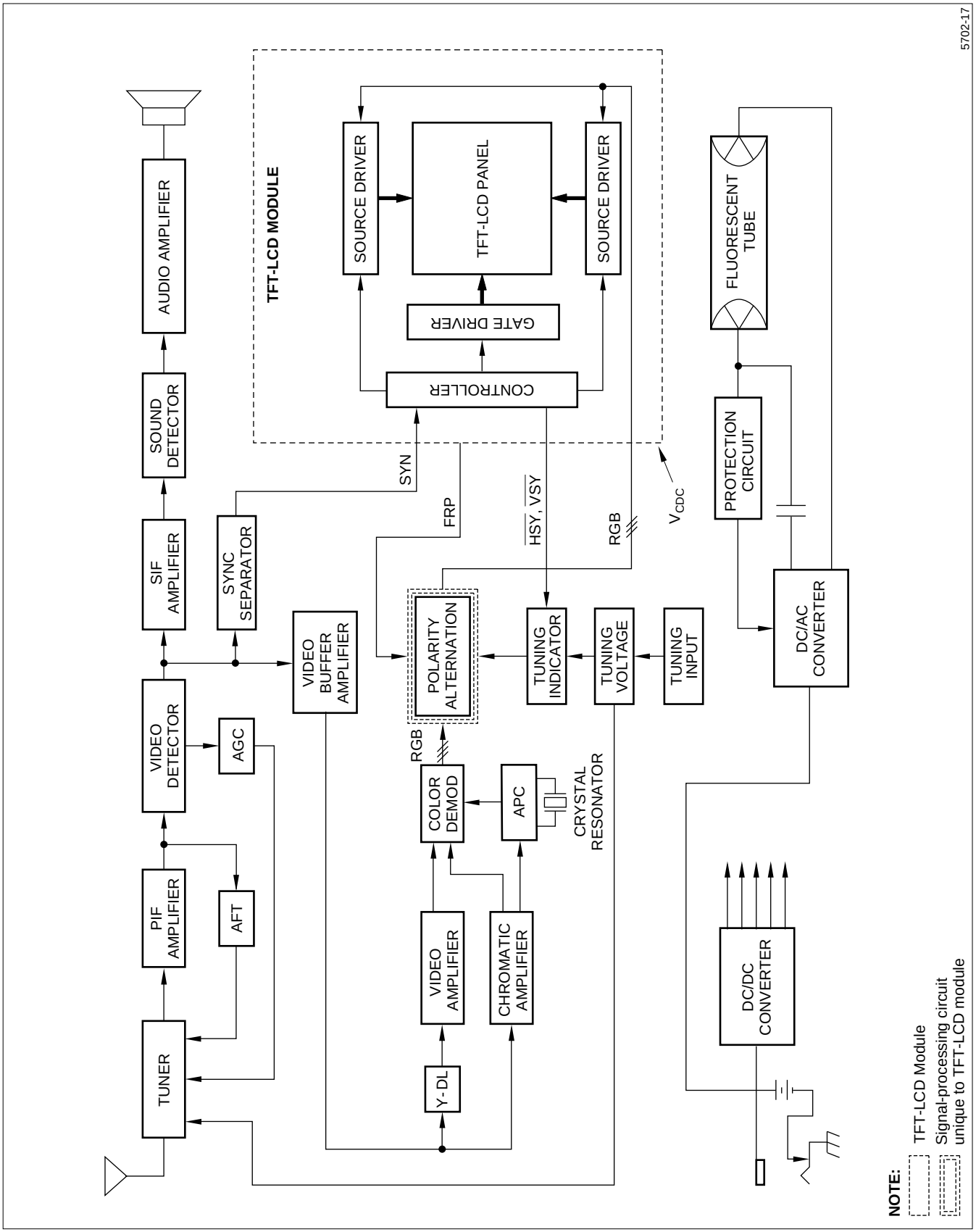



**Figure 15. Block Diagram of TFT-LCD TV Set**

## ADJUSTING METHOD OF OPTIMUM COMMON ELECTRODE DC BIAS VOLTAGE

To obtain optimum DC bias, photoelectric devices are very effective, and the accuracy is within 0.1 V. (In the visual examination method, the accuracy is about 0.5 V because of the difference among individuals.)

To gain optimum common electrode DC bias voltage, there are two methods which use photoelectric devices. The value of optimum DC bias voltage is the same in both methods:

- Measurement of Flicker: DC bias voltage is adjusted so as to minimize NTSC: 60 Hz (30 Hz), PAL: 50 Hz (25 Hz) flicker.
- Measurement of Contrast: DC bias voltage is adjusted so as to minimize the photoelectric output voltage.

### Measurement of Flicker

Photoelectric output voltage is measured by an oscilloscope in a system similar to that shown in Figure 16.

DC bias voltage must be adjusted to minimize the NTSC: 60 Hz (30z), PAL: 50 Hz (25 Hz) flicker with DC bias voltage changing slowly (Figure 17).

### Measurement of Contrast

Photoelectric output voltage is measured by oscilloscope or X-Y recorder by using the system in Figure 16. Common electrode DC bias voltage must be adjusted to minimize the photo-electric output voltage with DC bias voltage changing slowly (Figure 18).

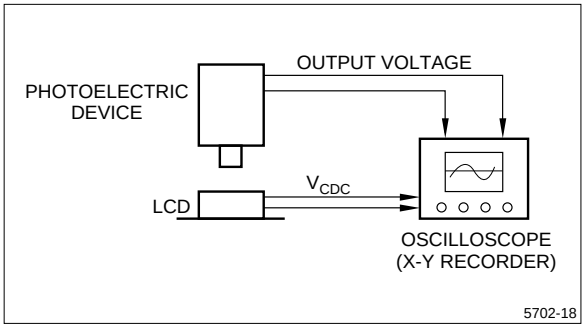



**Figure 16. Measurement System**

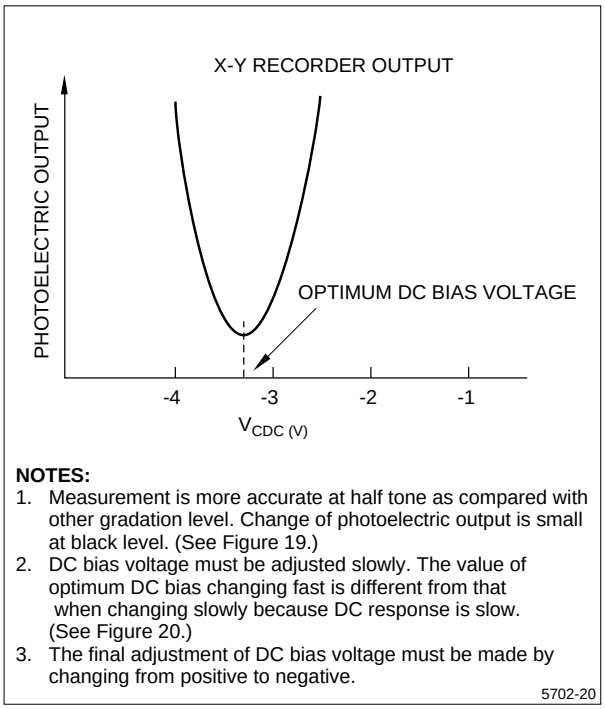



**Figure 18. Optimum Common Electrode DC Bias Voltage By Measurement of Contrast**

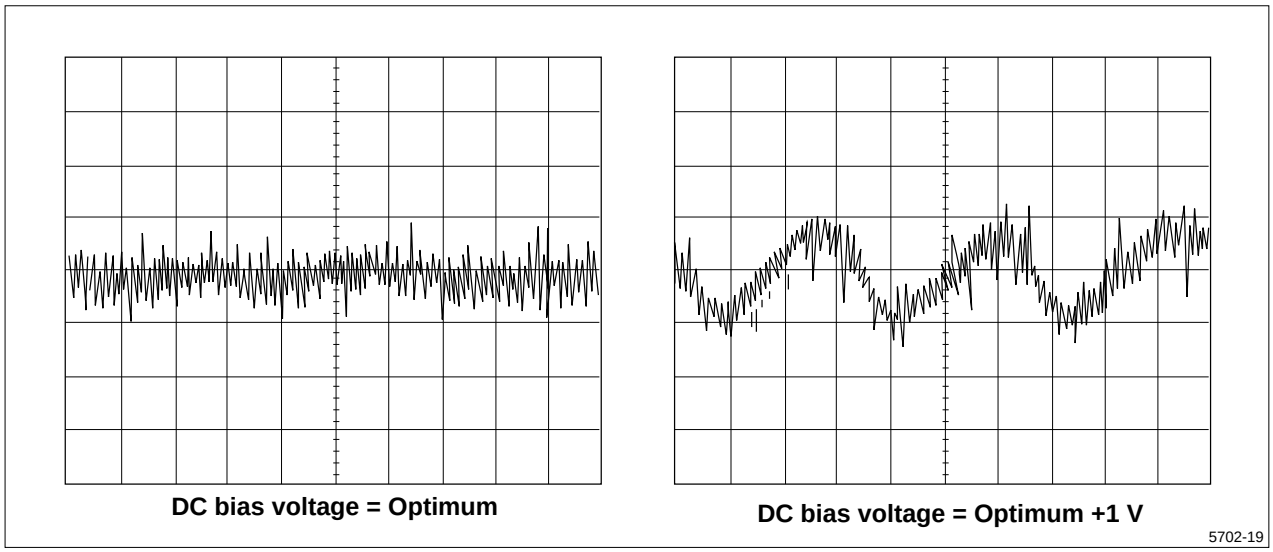
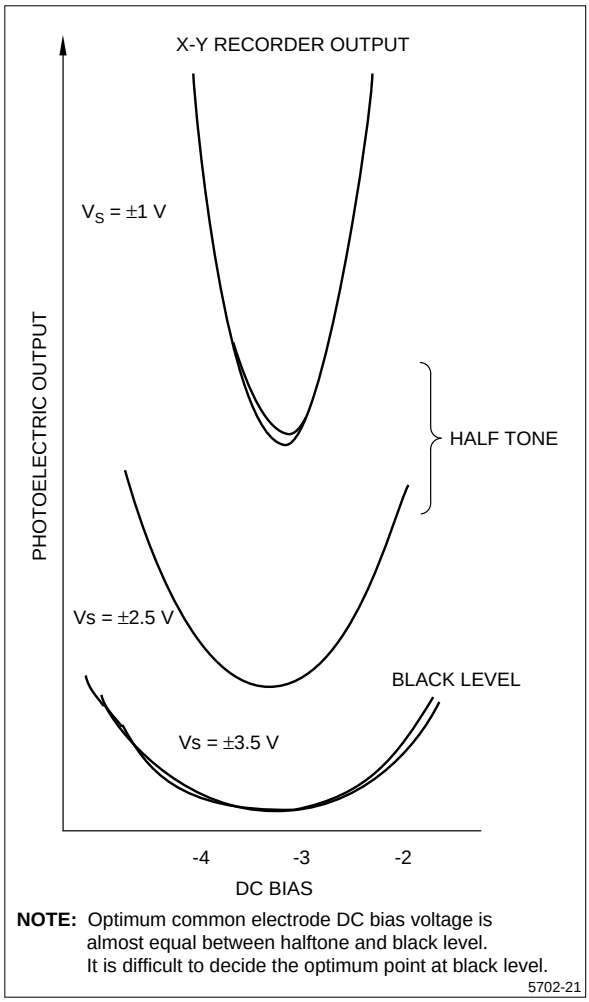



**Figure 17. Waveform of Flicker**




**NOTE:** Optimum common electrode DC bias voltage is almost equal between halftone and black level. It is difficult to decide the optimum point at black level.

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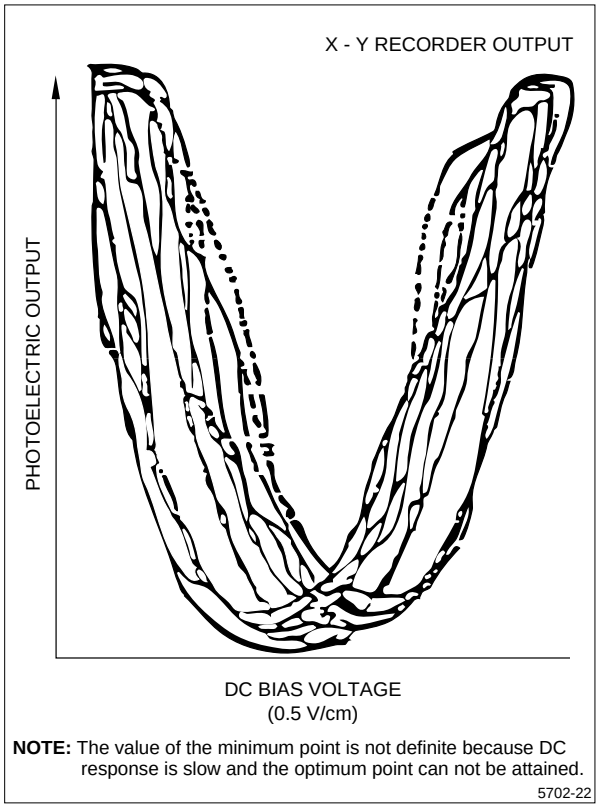
**Figure 19. Relation Between Gradation Level and DC Bias Voltage**




**NOTE:** The value of the minimum point is not definite because DC response is slow and the optimum point can not be attained.

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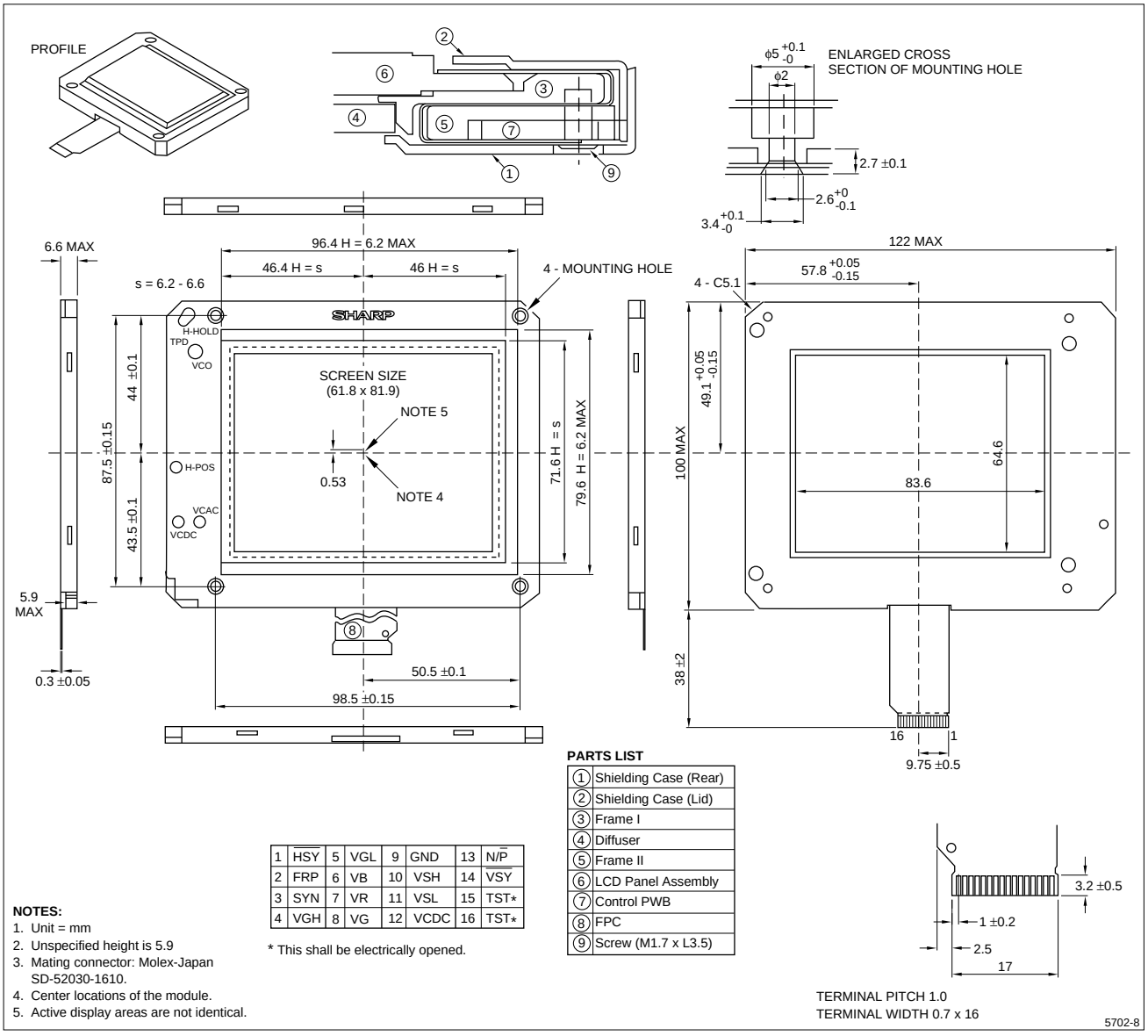
**Figure 20. Output Voltage With DC Bias Voltage Changing Fast**

## OUTLINE DIMENSIONS




**PARTS LIST**

| | |
|---|---|
| ① | Shielding Case (Rear) |
| ② | Shielding Case (Lid) |
| ③ | Frame I |
| ④ | Diffuser |
| ⑤ | Frame II |
| ⑥ | LCD Panel Assembly |
| ⑦ | Control PWB |
| ⑧ | FPC |
| ⑨ | Screw (M1.7 x L3.5) |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | $\overline{HSY}$ | 5 | VGL | 9 | GND | 13 | N/$\overline{P}$ |
| 2 | FRP | 6 | VB | 10 | VSH | 14 | $\overline{VSY}$ |
| 3 | SYN | 7 | VR | 11 | VSL | 15 | TST* |
| 4 | VGH | 8 | VG | 12 | VCDC | 16 | TST* |

* This shall be electrically opened.

**NOTES:**
1. Unit = mm
2. Unspecified height is 5.9
3. Mating connector: Molex-Japan SD-52030-1610.
4. Center locations of the module.
5. Active display areas are not identical.